

161

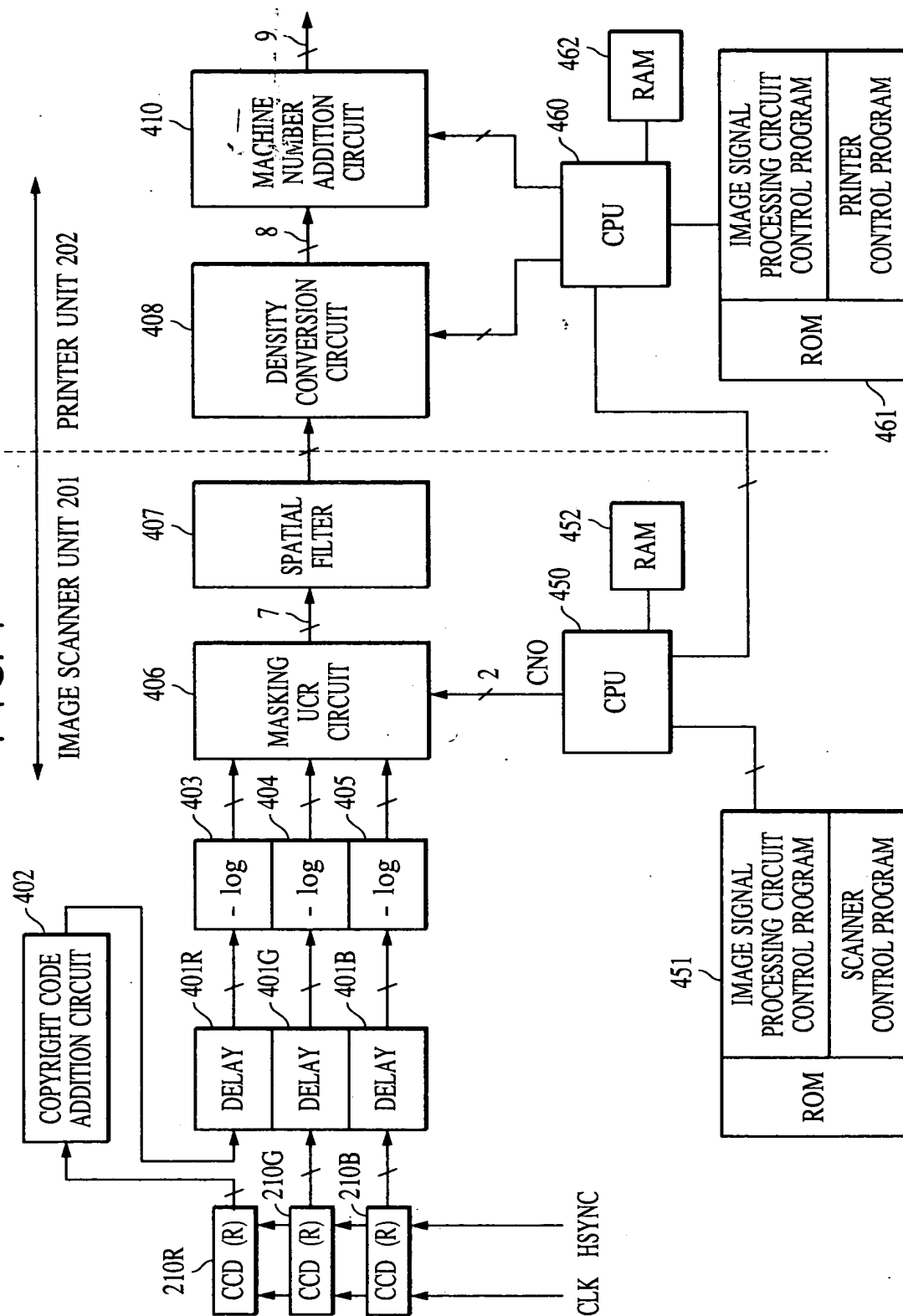


FIG. 2

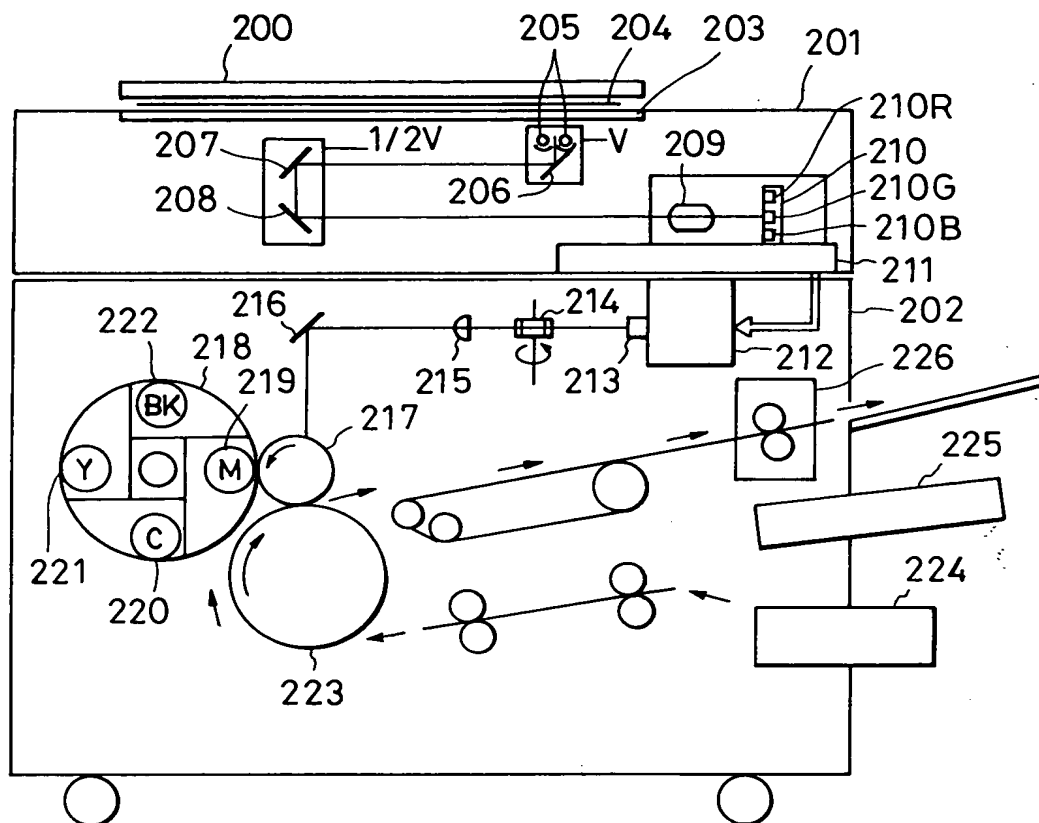


FIG. 3

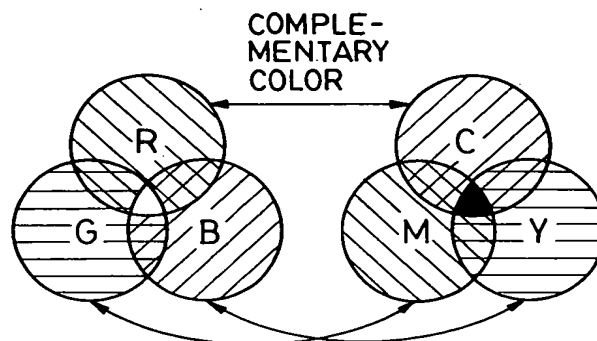


Figure 1 is a block diagram of a video signal processing circuit. The circuit includes two 8-bit registers (901, 902) for Q8~6 and Q5~0, a 3-bit register (903) for A11~6 and A5~0, a D-type flip-flop (905), a 3-bit register (904), a 3-bit register (906), a 3-bit register (911), and a 3-bit register (912). The circuit is controlled by VSYNC, HSYNC, and CLK signals. The output is V1.

CONFIDENTIAL

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
RAFTSMAN		

FIG. 7

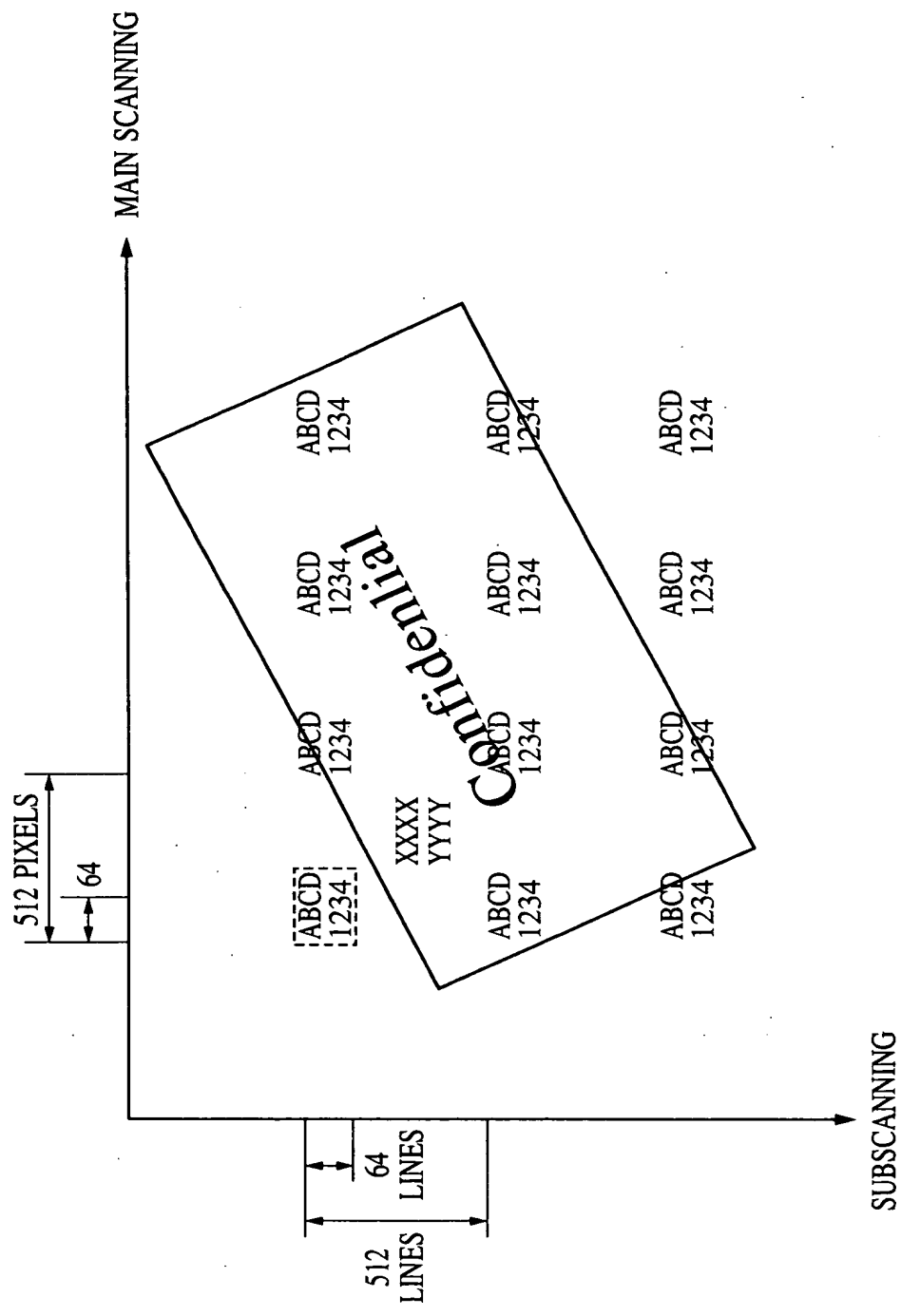
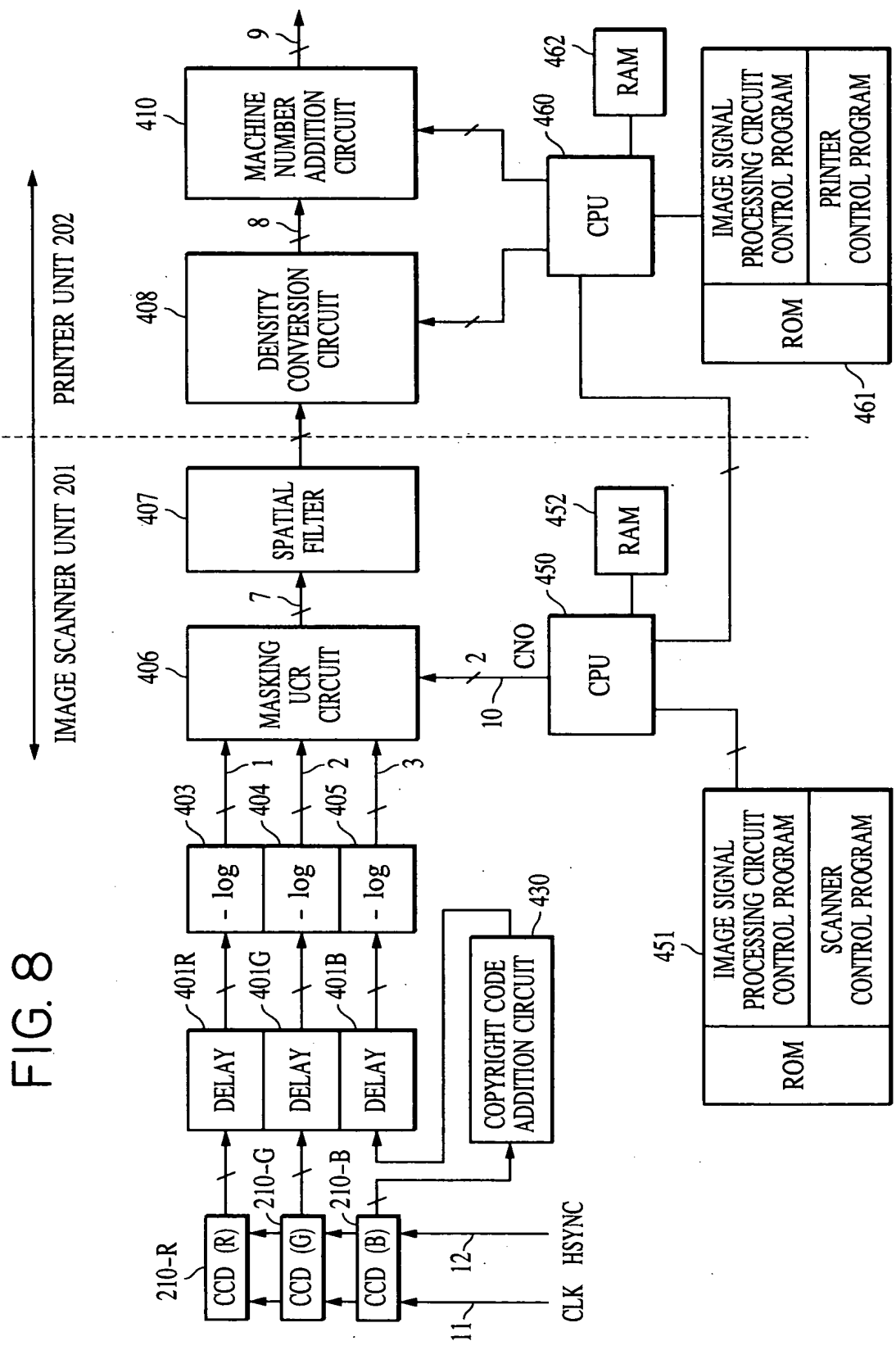


FIG. 8



66670-CT06260

APPROVED	O.G. FIG.	
BY	GLASS	BOUCLAGS
CRAFTSMAN		

FIG. 9

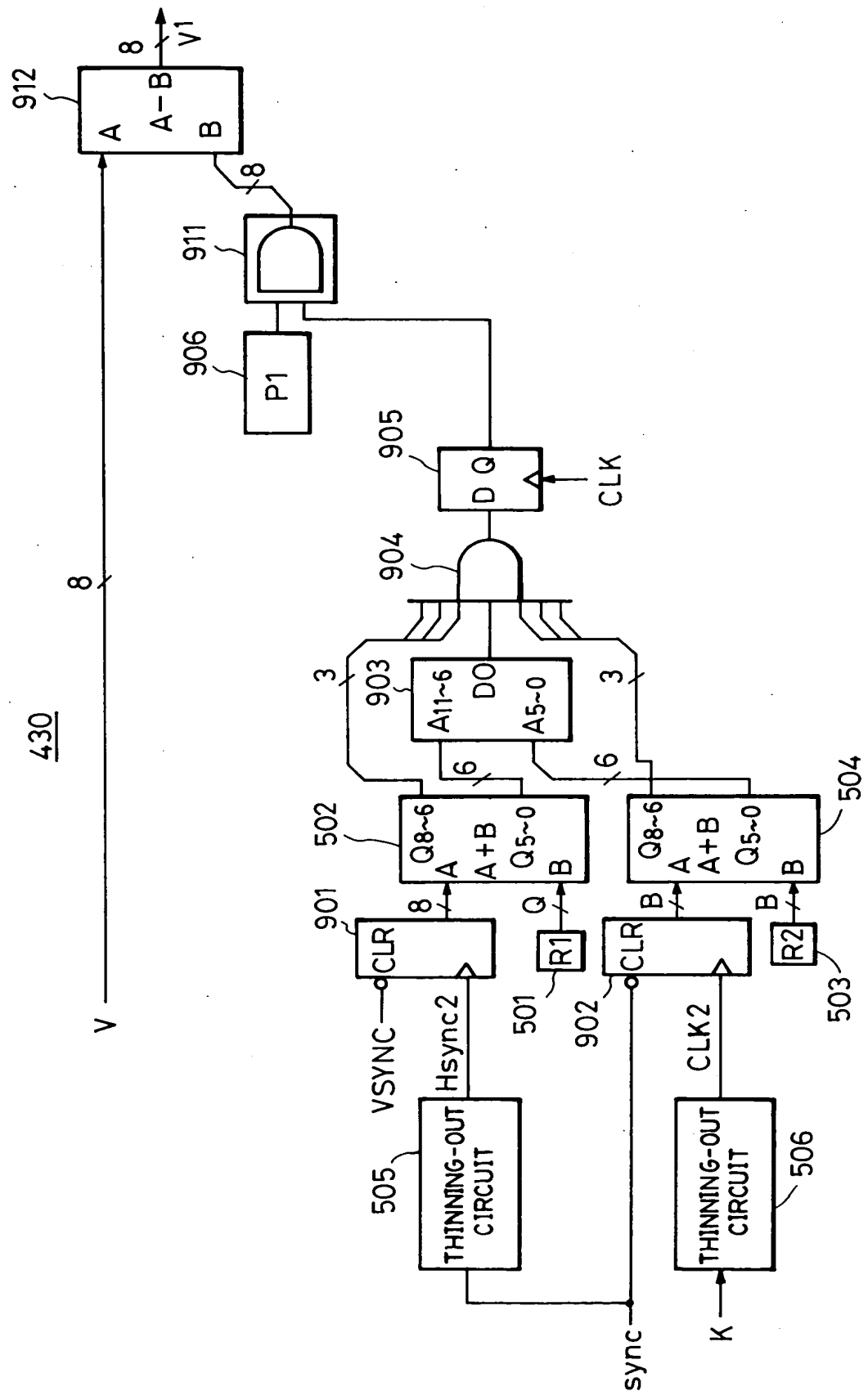


FIG. 10

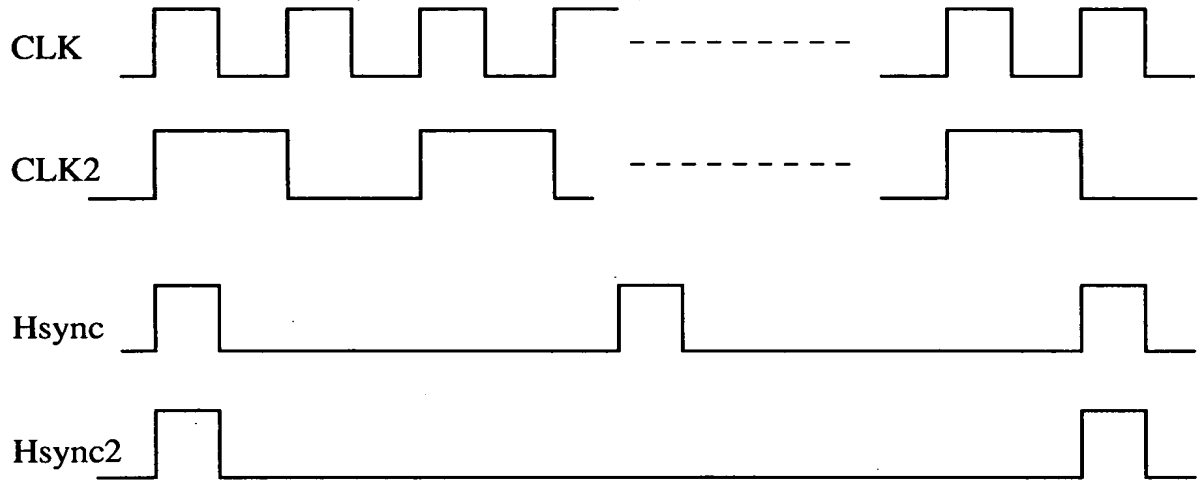


FIG. 11

1001
 A B C D
 1 2 3 4
 1002
 XXXX
 YYYY

FIG. 12

